REMARKS

I. CLAIM STATUS

Claims 1-34 remain pending.

II. REJECTIONS UNDER 35 U.S.C. § 112

Claim 3 stands rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The examiner asserts that the specification fails to describe the subject matter of claim 3 in such a way as to reasonably convey to one skilled in the art that the inventors possessed the claimed invention. Specifically, the examiner asserts that the specification fails to disclose "that an owner processor is capable of executing multiple threads concurrently." Applicants respectfully traverse.

Applicants first note that claim 3 is an original claim, i.e., it was present in the originally filed application, and hence it is part of the original specification. (*In re Gardner*, 178 USPQ 149, 149 (C.C.P.A. 1973) ("Under these circumstances, we consider the original claim in itself adequate "written description" of the claimed invention. It was equally a "written description" whether located among the original claims or in the descriptive part of the specification.").)

Applicants further note that the descriptive text also includes various teachings of multi-threading processors. See, e.g., the example in paragraph 16: "In a multithreaded system where multiple programs can execute simultaneously on the same processor, this can severely impact performance of the system. As an example, ..." See also paragraph 19, which begins "According to an exemplary embodiment, each processor preferably includes a Load Lock register associated with each program thread. ... ."

For at least these reasons, applicants maintain that this rejection of claim 3 is improper.

III. REJECTIONS UNDER 35 U.S.C. § 102

Claims 1, 2, 13, 14, 16, 24 and 25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Pat. No. 5,887,138, hereinafter "Hagersten." "To anticipate a claim, the reference must teach every element of the claim." MPEP 2131. Applicants respectfully traverse these rejections because the cited art fails to teach or suggest every element of the claims.

For example, independent claim 1 recites "wherein said Owner processor may displace the exclusive copy of said memory block, and return said displaced copy of said memory block to said Home processor with a signal indicating that said Owner processor remains a sharer of said memory block." **To emphasize and clarify, the processor is able to displace data from memory while maintaining a role that it does not in fact have, i.e., the role of a processor that continues to hold a copy of data in memory.** No such teaching can be found in the cited art.

The examiner cites c.13, ℓ21-39, as teaching the cited limitation, but this cite is to a paragraph that defines coherency states. Applicants fear that the examiner may be mistakenly mixing definitions of different coherency states. The paragraph states in part:

> In one embodiment, the coherency states employed by computer system 10 are **modified**, **owned**, **shared**, and **invalid**. The **modified state** indicates that the SMP node 12 has updated the corresponding coherency unit. ... [W]hen the modified coherency unit is discarded by the SMP node 12, the coherency unit is stored back to the home node. The **owned state** indicates that the SMP node 12 is responsible for the coherency unit, but other SMP nodes 12 may have shared copies. Again, when the coherency unit is discarded by the SMP node 12, the coherency unit is stored back to the home node. The **shared state** indicates that the SMP node 12 may read the coherency unit but may not update the coherency unit without acquiring the owned state. ... Finally, the **invalid state** indicates that the SMP node 12 does not have a copy of the coherency unit. (emphasis added)

The cited reference does not here or elsewhere teach or suggest that when a processor displaces data from memory, it assumes a role as a sharer of the data. For at least this reason, independent claim 1 and its dependent claim 2 are allowable over the cited art.

Independent claim 13 recites "displacing said copy of said memory block from said cache memory ... [and] transmitting a message to said Home processor relinquishing exclusive control of said memory block, while indicating that said Owner processor should still be deemed a sharer of said memory block." The examiner relies on the previous cite from Hagersten as teaching this limitation. However, as explained above, the cited portion of Hagersten merely defines different coherency states. No teaching or suggestion can be found of retaining a role as sharer after having displaced the data from memory. For at least this reason, independent claim 13 and its dependent claims 14 and 16 are allowable over the cited art.

Independent claim 24 recites "wherein said second processor may displace the exclusive copy of said memory block ... [and transmit] a signal to said first processor indicating that said second processor relinquishes exclusive control of said memory block but should remain a sharer of said memory block." The examiner relies on the previous cite from Hagersten as teaching this limitation. However, as explained above, the cited portion of Hagersten merely defines different coherency states. No teaching or suggestion can be found of retaining a role as sharer after having displaced the data from memory. For at least this reason, independent claim 24 and its dependent claim 25 are allowable over the cited art.

IV. REJECTIONS UNDER 35 U.S.C. § 103

Claims 3 and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten in view of U.S. Pat. No. 6,438,671, hereinafter "Doing." Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten in view of U.S. pat. No. 6,425,050, hereinafter "Beardsley." Claims 4, 17 and 27 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten in view of Doing and further in view of U.S.

Pat. No. 5,937,199, hereinafter "Temple." Claims 5-7, 18, 19, 28 and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten in view of Doing and Temple and further in view of U.S. Pub. No. 2001/0010068, hereinafter "Michael." Claims 8-12, 20-23 and 30-34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hagersten in view of Doing, Temple, Michael and Beardsley. Applicants respectfully traverse these rejections because the cited art fails to teach or suggest each limitation of the claims, as is required for a rejection of this type. *See* MPEP § 2142.

In each of the foregoing rejections, the examiner relies on Hagersten as teaching each limitation in the independent claims. As explained in the preceding section, Hagerston fails to teach or suggest each such limitation. Moreover, the other cited references similarly fail to teach or suggest the above-quoted limitations of the independent claims. For at least this reason, claims 3, 4, 5-7, 8-12, 15, 17, 18, 19, 20-23, 26, 27, 28, 29, and 30-34 are allowable over the cited references.

V. CONCLUSION

In the course of the foregoing discussions, applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited art which have yet to be raised, but which may be raised in the future.

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including

fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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